CLAIMS

What is claimed is:

1. An interconnect, comprising:

a semiconductor substrate having opposing surfaces, including:

a first insulated conductor for transmitting signals;

a second insulated conductor for transmitting signals; and

a third conductor substantially surrounding and electrically insulated from the first and second insulated conductors, wherein:

capacitance between the first insulated conductor and the third conductor is substantially equivalent to capacitance between the second insulated conductor and the third conductor; and

the first and the second insulated conductors are disposed between the opposing surfaces of the semiconductor substrate.

2. The interconnect as described in claim 1, wherein capacitance is substantially equivalent between:

the first insulated conductor and the semiconductor substrate; and

the second insulated conductor and the semiconductor substrate.

3. The interconnect as described in claim 1, wherein the shape of each of the third conductor, the first insulated conductor, and the second insulated conductor is such that electromagnetic interference encountered by the third conductor is symmetrically distributed to the first conductor and the second conductor .

4. The interconnect as described in claim 1, wherein the third conductor shields the first insulated conductor and the second insulated conductor from at least a portion of electromagnetic interference provided within the semiconductor substrate.

5. The interconnect as described in claim 1, wherein capacitance

between the first insulated conductor and the third conductor, and between the second insulated conductor and the third conductor, is substantially equivalent so that the first insulated conductor and the second insulated conductor are exposed to corresponding amounts of electromagnetic interference.

6. An apparatus, comprising:

a first capacitor including a first conductor and a second conductor, the second conductor disposed within the first conductor, wherein:

the second conductor transmits a signal;

a first insulator is disposed between the first conductor and the second conductor; and

the first and second conductors are disposed in a semiconductor substrate generally perpendicular to a plane of the semiconductor substrate;

a second capacitor including the first conductor and a third conductor, the third conductor disposed within the first conductor, wherein:

the third conductor transmits a signal;

the first insulator is disposed between the first conductor and the third conductor; and

the first and third conductors are disposed in the semiconductor substrate generally perpendicular to the plane of the semiconductor substrate;

a third capacitor including a semiconductor substrate and the first conductor, wherein a second insulator is disposed between the semiconductor substrate and the first conductor;

wherein capacitance of the first capacitor and the third capacitor is substantially equivalent to capacitance of the second capacitor and the third capacitor.

7. The apparatus as described in claim 6, wherein positioning of the second conductor and the third conductor is symmetrical with respect to the first conductor.

8. The apparatus as described in claim 6, wherein corresponding portions of the second conductor and the third conductor are exposed to corresponding amounts of electromagnetic interference from the first conductor.

9. The apparatus as described in claim 6, wherein capacitance of the first capacitor and the second capacitor is substantially equivalent.

10. A MicroElectroMechanical system (MEMS), comprising:

a first conductor for transmitting a signal;

a second conductor for transmitting a signal;

a first insulator substantially surrounding the first conductor and the second conductor;

a third conductor which substantially surrounds the first conductor, the second conductor, and the first insulator;

a second insulator substantially surrounding the third conductor; and

a semiconductor substrate having opposing surfaces, wherein:

capacitance of a path from the semiconductor substrate through the third conductor to the first conductor is substantially equivalent to capacitance of a path from the semiconductor substrate through the third conductor to the second conductor; and

the first and second conductors are defined between the opposing surfaces.

11. The MicroElectroMechanical system as described in claim 10, wherein electromagnetic interference encountered by the third conductor is symmetrically distributed to the first conductor and the second conductor.

12. The MicroElectroMechanical system as described in claim 10, wherein the third conductor shields the first conductor and the second conductor from at least a portion of electromagnetic interference encountered from the semiconductor substrate.

13. A system, comprising:

a source device providing a differential signal;

an interconnect communicatively coupled to the source device and defined between opposing surfaces of a semiconductor substrate, wherein the interconnect includes

a first conductor transmitting a first portion of the differential signal,

a second conductor transmitting a second portion of the differential signal, and

a third conductor which substantially surrounds the first conductor and the second conductor, wherein the third conductor distributes electromagnetic interference received by the third conductor so that the first conductor and the second conductor receive substantially equivalent amounts of the distributed electromagnetic interference; and

a receiving device communicatively coupled to the interconnect, the receiving device receives the first portion including the exposed electromagnetic interference from the first conductor and the second portion including the exposed electromagnetic interference from the second conductor, wherein the receiving device references the first portion with the second portion to remove the distributed electromagnetic interference.

14. The system as described in claim 13, wherein the source device is disposed on a first layer of a MicroElectroMechanical system (MEMS) structure, the interconnect is disposed on a second layer of a MEMS structure and the receiving device is disposed on a third layer of a MEMS structure, wherein the second layer is disposed between the first layer and the third layer.

15. The system as described in claim 13, wherein the source device is disposed on a first side of a semiconductor substrate, the receiving device is disposed on an opposing side of the semiconductor substrate, and the interconnect is disposed through the semiconductor substrate.

16. The system as described in claim 13, wherein the source device is configured as at least one of a MEMS device and an electronic device.

17. The system as described in claim 13, wherein the receiving device is configured as at least one of a MEMS device and an electronic device.

18. An electronic device comprising:

an interconnect having:

a first conductive path for transmitting a signal;

a second conductive path for transmitting a signal;

a first insulator substantially surrounding the first conductive path and the second conductive path;

a shield which substantially surrounds the first conductive path, the second conductive path, and the first insulator; and

a second insulator substantially surrounding the shield; and

a semiconductor substrate adjacent to the shield such that capacitance from the semiconductor substrate to the shield to the first conductive path is substantially equivalent to capacitance from the semiconductor substrate to the shield to the second conductive path, wherein the interconnect is disposed vertically in the semiconductor substrate.

19. The electronic device as described in claim 18, wherein at least one of the first insulator and the second insulator are formed from a dielectric material.

20. The electronic device as described in claim 18, wherein electromagnetic interference encountered by the shield is distributed to the first conductive path and the second conductive path in a substantially symmetrical manner.

21. The electronic device as described in claim 18, wherein the shield shields the first conductive path and the second conductive path from at least a

portion of electromagnetic interference provided within the semiconductor substrate.

22. The electronic device as described in claim 18, wherein a first portion of a differential signal is transmitted on the first conductive path and a second portion of the differential signal is transmitted on the second conductive path.

23. An interconnect for transmitting a signal comprising:

a first insulated conductor disposed within a semiconductor substrate;

a second insulated conductor disposed within the semiconductor substrate; and

a third conductor disposed within the semiconductor substrate and substantially surrounding the first and second insulated conductors so as to be symmetrical with respect to the first and second insulated conductors, wherein the third conductor is disposed perpendicular to a plane of the substrate.

24. The interconnect as described in Claim 23, further comprising opposing ends of the interconnect between which the signal is transmitted.

25. The interconnect as described in Claim 23, further comprising a dielectric electrically insulating and surrounding the third conductor.

26. An interconnect for transmitting a signal comprising:

a plurality of insulated conductors disposed within a semiconductor substrate; and

a shield disposed within the semiconductor substrate, the shield substantially surrounding the plurality of insulated conductors, wherein each of the insulated conductors receives a distribution of substantially equivalent amounts of EMI.

27. The interconnect as described in Claim 26, further comprising

opposing ends of the interconnect between which the signal is transmitted.

28. The interconnect as described in Claim 26, further comprising a dielectric electrically insulating and surrounding the third conductor.

29. A semiconductor device, comprising:

a first conductor for transmitting a signal, the first conductor disposed between opposing surfaces of a semiconductor substrate;

a second conductor for transmitting a signal, the insulated conductor disposed between the opposing surfaces of the semiconductor substrate; and

a third conductor disposed within the semiconductor substrate which substantially surrounds the first conductor and the second conductor,

wherein capacitance of the first conductor and the third conductor through configuration of corresponding surfaces areas of the first conductor and the third conductor, positioning the first conductor with respect to the third conductor, and resistance between the first conductor and the third conductor is substantially equivalent to capacitance of the second conductor and the third conductor through configuration of corresponding surfaces areas of the second conductor and the third conductor, positioning the second conductor with respect to the third conductor, and resistance between the second conductor and the third conductor.

30. A semiconductor device, comprising:

a first means for conducting a signal through a semiconductor substrate;

a second means for conducting a signal through the semiconductor substrate; and

means, substantially surrounding the first conducting means and the second conducting means, for symmetrically distributing encountered electromagnetic interference to the first conducting means and the second conducting means.

31. The semiconductor device as defined in claim 30, wherein:

the means for symmetrically distributing encountered electromagnetic interference is symmetrical with respect to the first and second means.

32. The semiconductor device as defined in claim 30, wherein the first and second means are symmetrical about a plane therebetween.

33. A method, comprising:

in an interconnect disposed between opposing surfaces of a semiconductor substrate, the interconnect having a first conductor and a second conductor, the first and second conductors disposed within a third conductor,

encountering electromagnetic interference with the third conductor; and

symmetrically distributing the encountered electromagnetic interference to the first conductor and the second conductor from the third conductor.

34. The method as described in claim 33, further comprising transmitting a differential signal through the interconnect, wherein a first portion of the differential signal is transmitted through the first conductor and a second portion of the differential signal is transmitted through the second conductor.

35. The method as described in claim 33, further comprising removing the distributed electromagnetic interference from the differential signal.

36. The method as described in claim 35, wherein the distributed electromagnetic interference is removed using common mode rejection.

37. The method as described in claim 33, further comprising shielding at least a portion of electromagnetic interference, originating from the semiconductor substrate and encountered by the third conductor, from the first conductor and the second conductor.

38. The method as described in claim 33, wherein at least a portion of the symmetrically distributed electromagnetic interference is incorporated in a

first portion of a differential signal transmitted through the first conductor and is incorporated in a second portion of the differential signal transmitted through the second conductor.

39. A method of making, comprising:

forming a first vertically oriented conductor from a semiconductor substrate;

forming a second vertically oriented conductor from the semiconductor substrate, the second conductor is formed adjacent to the first conductor; and

forming a third vertically oriented conductor from the semiconductor substrate, substantially surrounding the first conductor and the second conductor; and

forming an insulator which substantially surrounds the first conductor, the second conductor and the third conductor.

40. The method as described in claim 39, wherein the forming of the first conductor, the second conductor and the third conductor is performed by removing material from the semiconductor substrate.

41. The method as described in claim 39, the forming of the first conductor, the second conductor and the third conductor is performed by at least one of the group consisting of the following: deposition; etching; photolithography; micromachining; and any combination thereof.

42. The method as described in claim 39, wherein the forming of the first conductor, the second conductor and the third conductor is performed by creating a first channel and a second channel in the semiconductor substrate which define the first conductor, the second conductor and the third conductor.

43. The method as described in claim 39, wherein the forming of the insulator comprises depositing insulative material.

44. The method as described in claim 39, wherein the forming of the insulator comprises growing an oxide.

45. The method as described in claim 39, further comprising filling an opening of the insulator.

46. An interconnect formed by the process as described in claim 39.